REMARKS

In the June 16, 2005 Office Action claims 1-9 were rejected under 35 U.S.C. 103(a). Claims 10-12 have been added and thus, claims 1-12 remain in the case. No new matter has been added. The rejections are traversed below.

Rejections under 35 U.S.C. § 103

In item 6 on pages 3-9 of the June 16, 2005 Office Action, claims 1-9 were rejected under 35 U.S.C. 103(a) as being unpatentable over an article by Srivastava et al. entitled "Symbolic Approximation of Analog Circuits Using Sspice" (hereafter, Srivastava) in view of U.S. Patent 6,088,523 to Nabors et al. (hereafter, Nabors) and U.S. Patent 3,638,183 to Prögler et al. (hereafter, Prögler et al.).

The application is directed to wiring pattern analysis by analyzing RLC models and high-frequency element models in combination. Operations performed include conversion of RLGC lines to RLC lines and superimposing a skin resistance value on a DC resistance value (see page 24). Analysis delays are reduced by using a high-frequency element having a small high-frequency-element analysis delay time.

As discussed below, Srivastava, Prögler and Nabors either considered together or taken individually do not teach or suggest all of the limitations of the claimed invention. Thus, the applied art references of record cited in the June 16, 2005 Office Action, do not render the invention obvious.

Independent claim 1 recites "an analysis unit which executes an analysis ... using at least one of the elements corresponding to an integrated resistance value as a RLC model and using other elements ... as high-frequency element models" (claim 1, lines 17-19), where the "integrated resistance value" is obtained from "a second determination unit which integrates the resistance values starting with a resistance value having the smallest high-frequency element delay" (claim 1, lines 13-14). In other words, claim 1 recites circuit simulation analysis by merging RLGC lines into one RLGC line that is converted into a RLC model and using the RLC model and high-frequency element models in combination. In addition, a total of resistance values is calculated where each resistance value "is the sum of the DC resistance value and skin resistance value of each of the elements" (claim 1, lines 6-7).

On page 4, lines 11-14 of the Office Action, column 8, lines 19-25 of Nabors is cited as disclosing the "analysis unit" of claim 1. However, what was cited in Nabors describes simulation performance processing using a "reduced circuit having ... reduced quantities

associated with reduced circuit elements contained in the reduced circuit to obtain timing information about the electrical circuit" (column 8, lines 19-22). The terms "reduced quantities" and "reduced circuit element" apparently refer to the "reduced quantities ... arranged in a reduced RLCG line 280 having approximately the same performance as the original RLCG line 250" (column 7, lines 50-52). Nothing has been cited or found in Nabors suggesting conversion of an RLCG line into an RLC line to simplify the model used in the analysis, only combining elements of the RLCG line.

Also, nothing has been cited in either Srivastava or Nabors related to analyzing RLC and high-frequency element models in combination as recited in claim 1. Nabors is silent as to using other high-frequency element models. The only references to "frequency" in Nabors are the statement that in the equation in column 7, "s is a complex frequency" (column 7, line 52) and that "frequency dependent circuit element quantities can be manipulated just as the resistors, capacitors, inductors, and conductances" (column 26, lines 7-9). The only portions of Srivastava that were cited were "Sspice Element Definitions" on page 509 and use of a threshold at lines 22-26 on page 510 (discussed below). It is unclear where the "Sspice Element Definitions" are provided on page 509, and it is not understood how definitions of elements could teach or suggest the analysis recited in claim 1.

In addition, the portion of Nabors cited as disclosing that "resistance values corresponding to the elements" (claim 1, line 10) were sorted was column 3, line 60 to column 4, line 15. No mention of sorting anything has been found in this portion of Nabors.

Furthermore, combining Prögler with Srivastava and Nabors does not establish a case of *prima facie* obviousness because Prögler is non-analogous art and the thresholds disclosed therein are significantly different than the threshold values recited in claim 1. Srivastava and Nabors relate to high frequency signal analysis for circuit simulation and circuit design. In contrast, Prögler is directed to "signals ... fed into threshold value circuits at the receiver site and actuation or nonactuation of these circuits .... [in] data securing systems for data transmission over public telephone lines" (column 1, lines 3-15). The threshold values in Prögler relate to a threshold of the electric voltage applied in an electric circuit, and have nothing to do with the first threshold value recited in claim 1 which is compared with a total resistance value of summed a skin resistance superimposed on a DC resistance value for "elements corresponding to wiring patterns" (claim 1, lines 3-4) to maintain analysis precision of a high-frequency transmission in a circuit simulation environment, or the second threshold value recited in claim 1 which is compared to an integration result of resistance values (see, claim 1, lines 13-15). Prögler is

neither in the field of endeavor of nor reasonably pertinent to high frequency signal analysis related to circuit simulation and circuit design and the Office Action failed to establish a case of *prima facie* obviousness regarding the analysis unit recited in claim 1.

For the above reasons, claim 1 and claims 2-6 which depend therefrom are patentable over the applied art of record, Srivastava, Prögler and Nabors.

Claims 7-9 recite a program method and medium for performing circuit simulation analysis in a manner similar to claim 1. Therefore, it is submitted that claims 7-9 are patentable over the applied art of record for the reasons discussed above with respect to claim 1.

NEW CLAIMS

Newly added claims 10-12 further clarify the distinctions of the present invention over the applied art. Specifically, claim 10 recites "determining a total of resistance values, each resistance value being a sum of a direct current resistance value and a skin resistance value of a corresponding element in the circuit to be simulated" (claim 10, lines 2-4); "determining whether the total resistance value is less than a first threshold value" (claim 10, lines 5-6); "sorting the resistance values corresponding to the elements of the circuit ... to produce sorted resistance values" (claim 10, lines 7-9); and "determining an integration result, obtained by integrating as many as possible of the sorted resistance values that can be integrated without exceeding a second threshold value" (claim 10, last 3 lines). Therefore, it is submitted that claim 10 patentably distinguish over the applied art for reasons similar to those discussed above with respect to claim 1.

CONCLUSION

It is submitted that the references cited in the June 16, 2005 Office Action, taken individually or in combination, do not teach or suggest the features of the present claimed invention and for all of the reasons presented above, a case of *prima facie* obviousness has not been established in the Office Action.

There being no further outstanding objections or rejections, it is submitted that the claims 1-12 are in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 11/16/05

By: Richard A. Gollhofer
Richard A. Gollhofer
Registration No. 31,106

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501

CERTIFICATE OF FACSIMILE TRANSMISSION
I hereby certify that this correspondence is being transmitted via facsimile to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450
on November 16, 2005
STAAS & HALSEY
By: John L. Young
Date November 16, 2005